## Accelerated Life Testing of PV Arc-Fault Detectors

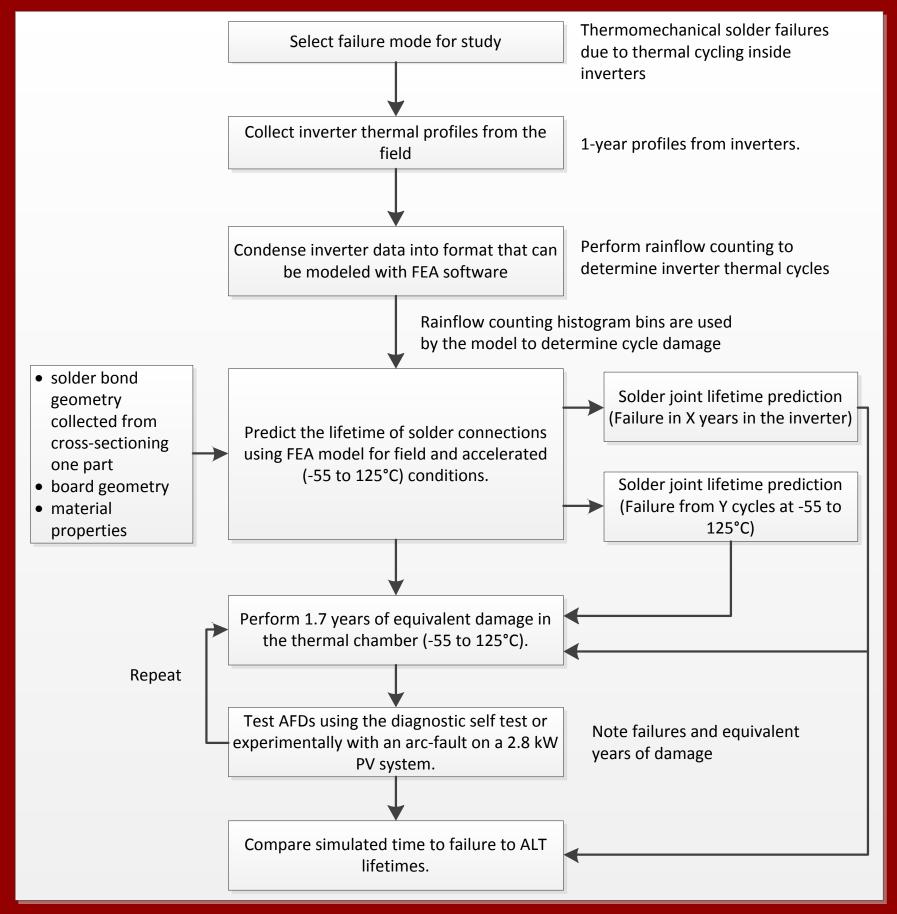
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As of 2011, the National Electrical Code® (NEC) has required arc-fault circuit interrupters (AFCIs) to be incorporated into photovoltaic (PV) systems to prevent fires. Some manufacturers are designing AFCIs to consist of arc-fault detectors (AFD) incorporated into inverters or combiner boxes in order to take advantage of the DC switching functionality of the existing hardware. Since AFCIs and AFDs are safety devices, it is critical to ensure the long-term functionality of AFD devices in these harsh environments. Sandia National Laboratories (SNL) has performed accelerated life tests on 10 AFDs. The devices were tested after being subjected to the thermal damage equivalent of 1.7-year increments in an inverter until 77.6 equivalent years of solder fatigue damage. 30% of the boards experienced component failures but there were no solder failures, indicating solder fatigue is not the primary failure mode. Based on these results, Sandia recommends an appropriate burn-in process for production of arc-fault devices.



# Solder Accelerated Life Testing Process

While the primary failure mode for AFD devices is unknown, microelectronic and discrete component solder bonds are known to fail on printed wiring boards as a result of harsh thermal environments. Specifically, thermomechanical solder fatigue failure is common in thermal cycling environments (e.g., automotive applications), so it was believed solder fatigue would be one of the leading causes of AFD failure in outdoor inverters which experience diurnal and seasonal cycling. To determine the lifetime of the solder joints, the following process was employed:

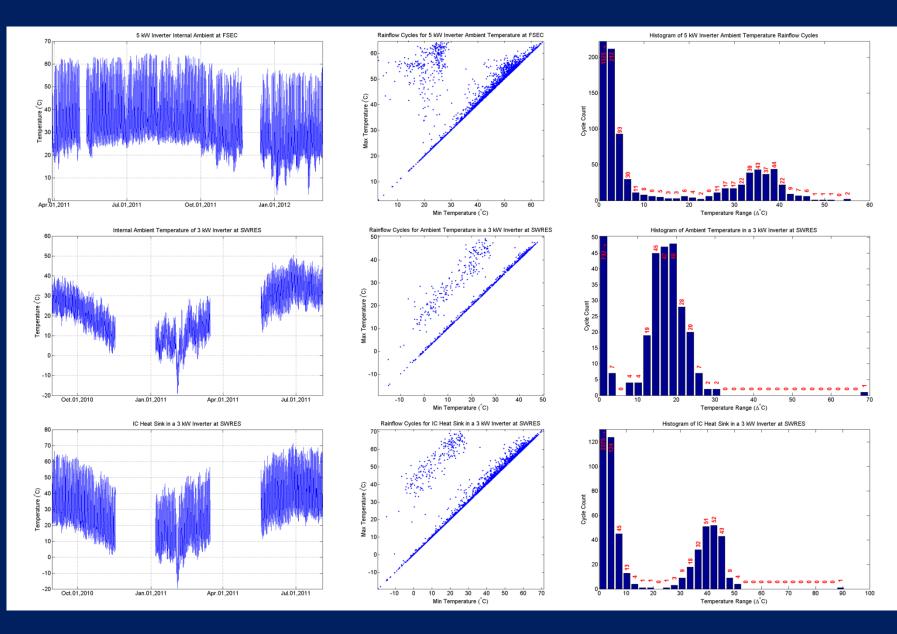


Process for determining the equivalent lifetime of the arc-fault detectors for the solder fatigue failure

### Modeling the Thermal Environment of an Inverter

To find the number of accelerated thermal cycles which produce 1-year of equivalent inverter exposure, a SNL-developed finite element analysis (FEA) code with Unified Creep Plasticity Damage (UCPD) material models for solder was run for rainflow count binned inverter thermal profiles and compared to simulations of -55 to 125°C cycles. The number of equivalent accelerated cycles was determined for the following thermal histories:

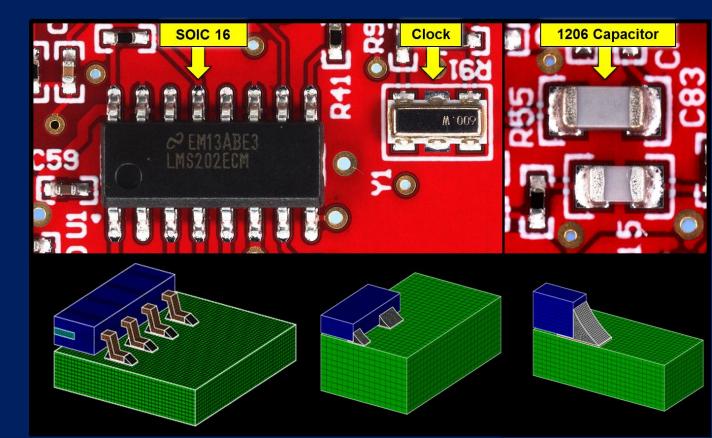
- 1. ambient temperature within a 5 kW inverter at the Florida Solar Energy Center (FSEC)
- 2. ambient temperature within a 3 kW inverter at the Southwest Region Experiment Station (SWRES) at the New Mexico State University in Las Cruces, NM.
- 3. integrated circuit heat sink temperature within a 3 kW inverter at SWRES (theoretical comparison only).



Thermal histories of three locations in PV inverters, associated rainflow matrices, and resulting histograms of rainflow counts.

### Solder Joint Failure Analysis

Solder fatigue damage calculations for the joints of the gull-wing 16-lead small outline integrated circuit (SOIC), 6-joint leaded ceramic chip carrier (LCCC) clock, and 1206 capacitor were performed.



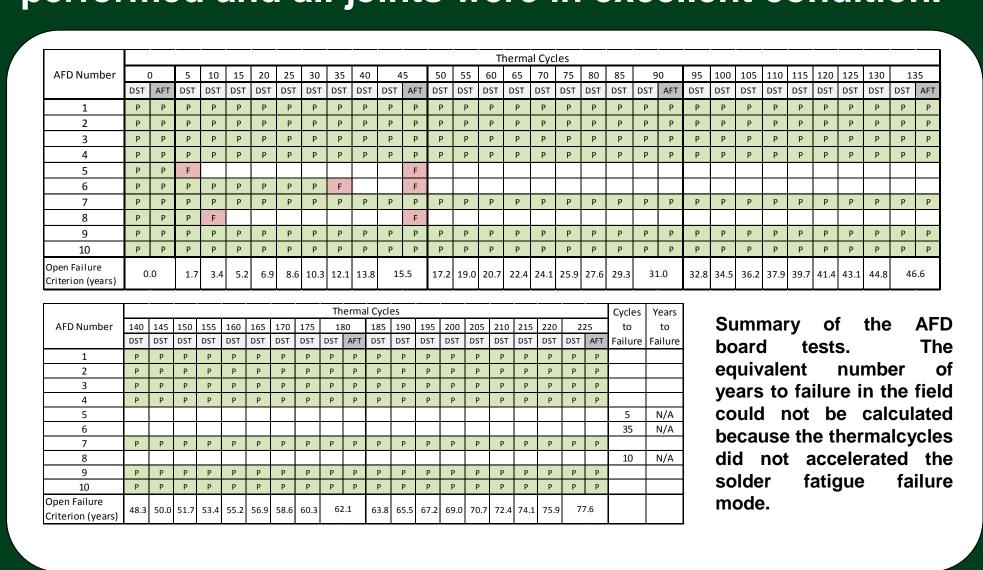
Calculations indicated that the fatigue damage rate was highest in the clock solder joints. The FSEC ambient inverter thermal history was the most damaging internal ambient environment, so it was used to find the expected life and equivalent number of accelerated life cycles.

Bin (ΔT)	Count	Crack Initiation Failure Criterion			50% Solder Crack Failure Criterion			Complete Crack (Open) Failure Criterion		
		Damage per cycle	Damage per history	Damage per year	Damage per cycle	Damage per history	Damage per year	Damage per cycle	Damage per history	Damage p year
4.482	335	5.52E-12%	1.85E-09%	2.19E-09%	2.08E-13%	6.98E-11%	8.28E-11%	1.04E-13%	3.49E-11%	4.14E-11
10.580	25	2.10E-06%	0.00005%	0.00006%	1.04E-07%	2.60E-06%	3.09E-06%	5.21E-08%	1.30E-06%	1.55E-06
16.086	11	0.00005%	0.00056%	0.00066%	4.65E-06%	0.00005%	0.00006%	2.15E-06%	0.00002%	0.000039
21.282	12	0.00028%	0.00337%	0.00400%	0.00003%	0.00036%	0.00043%	0.00001%	0.00016%	0.000209
27.953	34	0.00088%	0.03002%	0.03561%	0.00011%	0.00389%	0.00461%	0.00005%	0.00177%	0.002109
33.350	78	0.00216%	0.16811%	0.19942%	0.00028%	0.02167%	0.02572%	0.00013%	0.01016%	0.012069
38.323	124	0.00438%	0.54338%	0.64457%	0.00062%	0.07654%	0.09086%	0.00026%	0.03280%	0.038949
43.061	38	0.00811%	0.30807%	0.36544%	0.00115%	0.04368%	0.05185%	0.00047%	0.01784%	0.021189
48.113	8	0.01393%	0.11147%	0.13223%	0.00185%	0.01481%	0.01759%	0.00074%	0.00588%	0.006989
55.334	3	0.02258%	0.06773%	0.08035%	0.00278%	0.00833%	0.00989%	0.00106%	0.00319%	0.003799
Total	668	0.05237%	1.23277%	1.46233%	0.00682%	0.16934%	0.20101%	0.00273%	0.07183%	0.085279
Years to Failure in Field			68.4			497.5			1173	
Damage per -55 to 125°C Cycle			1.1700%			0.13333%			0.02941%	
Accelerated Cycles to Failure		85.5			750			3400		
Accelerated Cycles per 1 Year in Field		1.25			1.51			2.90		

Damage from rainflow cycle bins and calculations for equivalent damage from accelerated cycles for three crack-propagation failure criteria.

#### **Results and Discussion**

All 10 of the AFD boards were exposed to 225 thermal cycles. After every five cycles, the boards were tested using the internal diagnostic self test function; and after 45 cycles (15.5 years of equivalent solder damage using the 100% solder crack failure criteria), physical arc-fault tests were conducted at the Distributed Energy Technologies Laboratory at SNL. After all the accelerated cycles, there were no failures from solder fatigue. Rather, there were infant mortality failures of 30% of the AFDs; and therefore, the expected lifetimes of those parts could not be calculated using the FEA model. In all the failed boards, visual inspection of the solder joints was performed and all joints were in excellent condition.



#### **Conclusions:**

- 1. The on-board diagnostic self test function of the AFDs works well to indicate when the functionality of the boards is lost.
- 2. Solder fatigue is an unlikely AFD failure mode when installed in an inverter.
- 3. Since the AFD are required to operate for long periods of time in harsh environments, using a burn-in (stress screen) process to identify faulty components will be used in the future.





